A theoretical and experimental evaluation of surface roughness variation in trigate metal oxide semiconductor field effect transistors

M. R. Jiang, E. R. Hsieh, and Steve S. Chung

Department of Electronics Engineering and Institute of Electronics, National Chiao Tung University, Hsinchu 300, Taiwan

INTRODUCTION

The fluctuations of electric parameters in CMOS devices become more pronounced with scaling, and one of the most significant issues is the threshold voltage ($V_{th}$) fluctuation. There is a direct correlation between the gate current ($I_g$) fluctuation and the variation of oxide thickness. This is one of the reasons why the gate dielectric is the dominant factor of the gate leakage. However, no analytical or experimental study has been provided in the unique 3D structure of trigate.

THEORY AND METHODOLOGY

Bulk planar and trigate CMOS transistors were used in this work. The gate dielectric is the dominant factor of the gate leakage. However, no analytical or experimental study has been provided in the unique 3D structure of trigate.

RESULTS AND DISCUSSION

Experimentally, Fig. 4(a) shows that the smaller area is, the larger the fluctuation of the normalized gate current variation becomes. Then, variation of the oxide thickness can be calculated from the normalized $I_g$ variation by Eq. (2). As shown in Fig. 4(b), the variation of $T_{ox}$ increases as the device area decreases. Fig. 5 shows that the $SR$ of the device with 30 nm fin height is much larger than 10 nm ones, which indicates that the surface roughness of the sidewall for the device with 30 nm fin height is much worse. In Fig. 5, Curves of $I_g$, $T_{ox}$, $V_{th}$, and $V_{ds}$ are shown in Fig. 6(a), (b), (c), and (d), respectively. It was found that, at $L/W$ of 40/36 nm, the slope of $V_{th}$ versus $W_{total}$ is approximately equal to the slope of $V_{th}$ versus $W_{total}$ in Fig. 6(b).

REFERENCES